**DAILY ASSESSMENT FORMAT**

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| **Date:** | 29 May 2020 | **Name:** | Shreya poojary |
| **Course:** | Logic design | **USN:** | 4al16ec074 |
| **Topic:** | Analysis of clocked sequential circuits  **Digital clock design** | **Semester & Section:** | 8- B |
| **Github Repository:** | Shreya-test |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Report:** **ANALYSIS OF CLOCKED SEQUENTIAL CIRCUITS**    * Flip-flops have asynchronous inputs that are used to force the flip-flop to a particular state independently of the clock      * Input that sets the flip-flop to 1 is called preset or direct set. The input that clears the flip-flop to 0 is called clear or direct reset.      * When power is turned on in a digital system, the state of the flip-flops is unknown. The direct inputs are useful for bringing all flip-flops in the system to a known starting state prior to the clocked operation.      * The knowledge of the type of flip-flops and a list of the Boolean expressions of the combinational circuit provide the information needed to draw the logic diagram of the se­quential circuit. The part of the combinational circuit that gene rates external outputs is de­scribed algebraically by a set of Boolean functions called output equations. The part of the circuit that generates the inputs to flip-flops is described algebraically by a set of Boolean func­tions called flip-flop input equations (or excitation equations).      * The information available in a state table can be represented graphically in the form of a state diagram. In this type of diagram a state is represented by a circle and the (clock-triggered) transitions between states are indicated by directed lines connecting the circles.      * The time sequence of inputs, outputs, and flip-flop states can be enumerated in a state table (transition table). The table has four parts present state, next state, inputs and outputs.   Generally a sequential circuit with 'm' flip-flops and 'n' inputs needs 2m+n rows in the state table.  **Positive Edge Triggered D Flip-flop**   * When the reset input is 0 it forces output Q' to Stay at 1 which clears output Q to 0 thus resetting the flip-flop.      * Two other connections from the reset input ensure that the S input of the third SR latch stays at logic 1 while the reset input is at 0 regardless of the values of D and Clk.      * Function table suggests that:      * + When R = 0, the output is set to 0 (independent of D and Clk).      * + The clock at Clk is shown with an upward arrow to indi­cate that the flip-flop triggers on the positive edge of the clock.      * + The value in D is transferred to Q with every positive-edge clock signal provided that R = 1.   Positive Edge Triggered D Flip-flop **Analysis of T Flip-Flops**    * The circuit can be specified by the characteristic equations:      * + **Q(t+1) = T ⊕ Q = T'Q + TQ'** * The sequential circuit has two flip-flops A and B, one input x, and one output y and can be described algebraically by two input equations and an output equation * The state table for the circuit is listed below. The values for y are obtained from the out­put equation. The values for the next state can be derived from the state equations by substi­tuting TA and TB in the characteristic equations yielding:      * + **A(t + 1) = (Bx)' A + (Bx)A' = AB' + Ax' + A'Bx**      * + **B(t + 1) = x ⊕ B** |

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